ANALOG DEVICES

AN-397
APPLICATION NOTE

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Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence

by Niall Lyne

INTRODUCTION

The sensitivity of electronic components to transient electrical overstress events is a well-known problem, exacerbated by the continuing evolution of integrated circuits. Smaller geometries, increased circuit densities, and the limited area allotted to on-chip protection all tend to increase this sensitivity. In an effort to minimize costs in each particular segment of system implementation, the burden of transient protection is often shifted to other, less efficient means.

Techniques for protection from "zapping" depend on the stage of manufacture. During the manufacturing of integrated circuits and assembly of electronic equipment, protection is achieved through the use of well-known measures such as static dissipative table tops, wrist straps, ionized air blowers, antistatic shipping tubes, etc. These methods will be discussed only briefly here in relation to Electrostatic Discharge (ESD) protection. Likewise this application note is not addressed to precautionary measures employed during shipping, installation, or repair of equipment. Rather, the main thrust will be limited to protection aspects called upon during printed circuit board assembly, normal operation of the equipment (often by operating personnel who are untrained in preventative measures), and in service conditions where the transient environment may not be well characterized.

The transient environment varies widely. There are substantial differences among those experienced by, say, automotive systems, airborne or shipborne equipment, space systems, industrial equipment or consumer products. All types of electronic components can be destroyed or degraded.[1] Even capacitors, relays, connectors, printed circuit boards, etc., are susceptible, although their threshold levels are much higher than integrated circuits. Microwave diodes and transistors are among the most sensitive components. However, this application note will be restricted to standard linear integrated circuits because of their wide usage, and to limit the scope of coverage.

This application note will first review the nature of the threat to integrated circuits in an operating environment, and then briefly discuss overall device protection from the following: (1) *ESD* events caused by human handling, automatic board insertion equipment, etc., (2) *LATCH-UP* generated from power-up/down sequencing errors, floating ground(s) due to a loose edge connectors, etc., and finally, (3) *HIGH VOLTAGE TRANSIENTS* generated from a power supply, a defective circuit board, during circuit board troubleshooting, etc.

Electrostatic Discharge

Electrostatic discharge is a single, fast, high current transfer of electrostatic charge that results from:

- Direct contact transfer between two objects at different potentials, *or*
- A high electrostatic field between two objects when they are in close proximity.

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

The generation of static electricity caused by rubbing two substances together is called the triboelectric effect. Examples of sources of triboelectric electrostatic charge generation in a high RH (≈60%) environment include:

- Walking across a carpet ⇒ 1000 V–1500 V generated.
- Walking across a vinyl floor ⇒ 150 V–250 V generated.
- Handling material protected by clear plastic covers ⇒ 400 V–600 V generated.
- Handling polyethylene bags ⇒ 1000 V–1200 V generated.
- Pouring polyurethane foam into a box ⇒ 1200 V–1500 V generated.

- ICs sliding down an open antistatic shipping tube ⇒ 25 V–250 V generated.

Note: For low RH (<30%) environments, generated voltages can be >10× those listed above.

ESD Models

To evaluate the susceptibility of devices to simulated stress environments a host of test waveforms have been developed. The three most prominent of these waveforms currently in general use for simulating ESD events in semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). The test circuits and current waveform characteristics for these three models are shown in Figures 1 to 3. Each of these models represents a fundamentally different ESD event. Consequently, correlation between the test results for these models is minimal.

Human Body Model:[2]

Simulates the discharge event that occurs when a person charged to either a positive or negative potential touches an IC at a different potential.

RLC = 1.5 kΩ, ~0 nH, 100 pF.

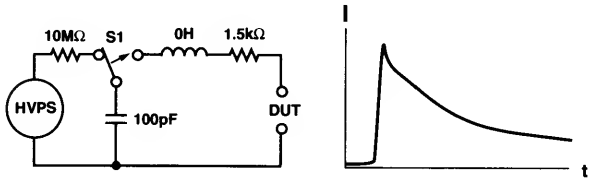

Figure 1. Human Body Model

Machine Model:

Japanese model based on a worst-case HBM.

RLC = 0 Ω, 500 nH, 200 pF.

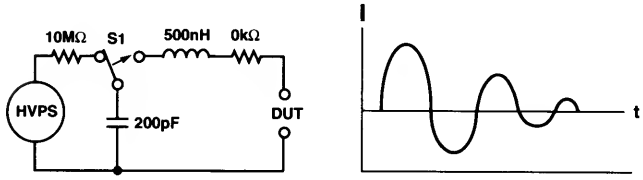

Figure 2. Machine Model

Charged Device Model:

Simulates the discharge that occurs when a pin on an IC charged to either a positive or negative potential contacts a conductive surface at a different (usually ground) potential.

RLC = 0 Ω, ~0 nH, 1 pF–20 pF.

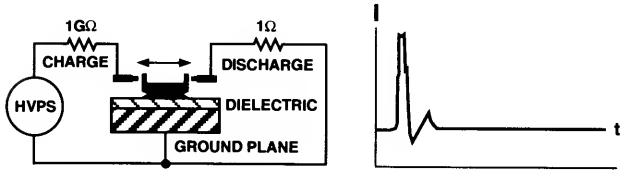

Figure 3. Charged Device Model

Comparison of HBM, MM, and CDM Waveforms

Figure 4 shows 400 V HBM, MM, and CDM discharge waveforms on the same current vs. time scale. These waveforms are of great use in predicting what failure mechanism may result on a particular device type due to ESD events simulated by one of these three models.

The rise time for the HBM waveform is <10 ns (typically 6 ns–9 ns), and this waveform decays exponentially towards 0 V with a fall time of >150 ns. MIL-STD-883[3] Method 3015 *Electrostatic Discharge Sensitivity Classification* requires a rise time of <10 ns and a delay time of 150 ± 20 ns (Method 3015 defines delay time as the time for the waveform to drop from 90% of the peak current to 36.8% of the peak current). The peak current for the HBM waveform is ≈400 V/1500 Ω or 0.267A. Although this peak current is much lower than that for 400 V CDM and MM events, the relatively long duration of the total HBM event results in a discharge of relatively high energy.

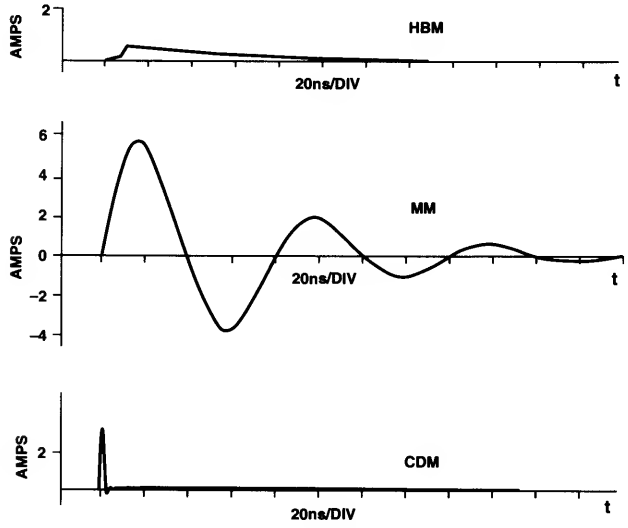

Figure 4. Relative Comparison of 400 V HBM, MM, and CDM Discharges

The MM waveform consists of both positive-going and negative-going sinusoidal peaks with peak magnitudes that decay exponentially. The initial MM peak has a rise time of ≈14 ns, i.e., only slightly greater than that of the single HBM peak. The total duration of the MM waveform is comparable to that for the HBM waveform. However, the peak current for the first peak of the 400 V MM event is ≈5.8 A, which is the highest of the three models. The next four peaks, though decreasing in current, still all have magnitudes of >1 A. These multiple high current peaks of substantial duration result in an overall discharge energy that is by far the highest of the three models because there is no current limiting; R = 0 Ω.

The CDM waveform corresponds to the shortest known real-world ESD event. The socketed CDM waveform has a rise time of 400 ps, with the total duration of the CDM event of ≈2 ns. The CDM waveform is essentially unipolar, although some slight ringing occurs at the end of the CDM event that results in some negative-going peaks.

With a 400 V charging voltage, a socketed CDM discharge will have a peak current of 2.1 A. However, the very short duration of the overall CDM event results in an overall discharge of relatively low energy.

Summary of ESD Models

Table I is a reference table that compares the most important characteristics of the three ESD simulation models.

Table I.

Model	HBM	MM	Socketed CDM
Simulate	Human Body	Machine	Charged Device
Origin	US Military Late 1960s	Japan 1976	AT&T 1974
Real World	Yes	Generally No	Yes
RC	1.5 kΩ, 100 pF	0 Ω, 200 pF	1 Ω, 1 pF–20 pF
Rise Time	<10 ns	14 ns*	400 ps**
I_{PEAK} at 400 V	0.27 A	5.8 A*	2.1 A**
Package Dependent	No	No	Yes
Leakage Recovery	No	No	Yes
Standard	MIL-STD-883 Method 3015	ESD Assoc. Standard S5.2; EIAJ Standard ED-4701, Method C-111	ESD Assoc. Draft Standard DS5.3

* These values are per ESD Association Standard S5.2. EIAJs standard ED-4701 Method C-111 includes no waveform specifications.
**These values are for the direct charging (socketed) method.

Prevention

When auditing a facility in which ESD protective measures will be taken, the following should be considered:[4]

- There must be a grounded workbench on which to handle static sensitive devices incorporating:
  a) Personal ground strap (wrist strap)
  b) Conductive trays or shunts, etc.
  c) Conductive work surface
  d) Conductive floor or mat
  e) A common ground point
- All steel shelving or cabinets used to store devices must be grounded.
- The relative humidity should be controlled; the desirable range is 40 to 60 percent. Where high relative humidity levels cannot be maintained, the use of ionized air should be used to dissipate electrostatic charges.
- All electrical equipment used in the area must be grounded.
- Prohibit the use of prime static generators, e.g., Scotch tape.
- Follow up with ESD audits at a minimum of three month intervals.
- Training: Keep in mind, the key to an effective ESD control program is "TRAINING." Training should be given to all personnel who come in contact with integrated circuits and should be documented for certification purposes, e.g., ISO 9000 audits.

Determining whether a device failed as a result of ESD or Electrical Overstress (EOS) can be difficult and is often best left to Failure Analysis Engineers. Typically ESD damage is less obvious than that of EOS when electrical analysis and internal visual analysis are performed. In the case of ESD, events of 1 kV or more (depending on the ESD rating of the device) can rupture oxides (inter layer dielectric of the die) and damage junctions in less than 10 ns (see Figure 6). Alternately, EOS conditions leading to 1 to 3 amps of current for a duration of ≥1 ms can cause sufficient self-heating of bond wires to fuse them. Such conditions can occur as a result of latch-up. Lower currents can cause rapid melting of chip metallization and other interconnect layers (see Figure 5).

Figure 5. Scanning Electron Microscope View of a Fused Metallization Site, as a Result of Electrical Overstress

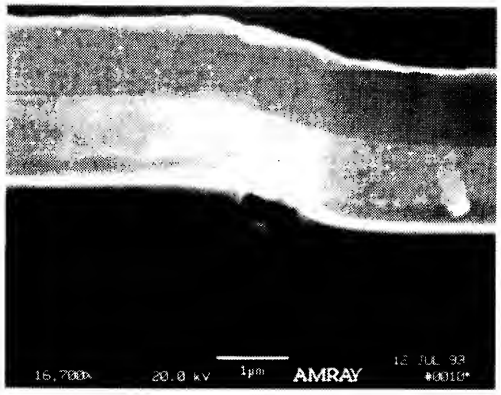

Figure 6. Scanning Electron Microscope Cross-Sectional View of a CDM ESD Site. This subsurface site could not be viewed from the surface with an optical microscope.

A quick analysis can be performed on site to evaluate if a device may have been overstressed or may have been subjected to an ESD event. In order to perform this analysis, to compare the pin-to-pin I/V results of the suspect device to those of a known good device, a curve tracer or similar equipment should be used. A typical set of I/V traces for a short circuit, open circuit or ESD leakage on a digital input pin (with reference to the V_{SS} supply pin) of a 12-bit DAC is shown in Figure 7.

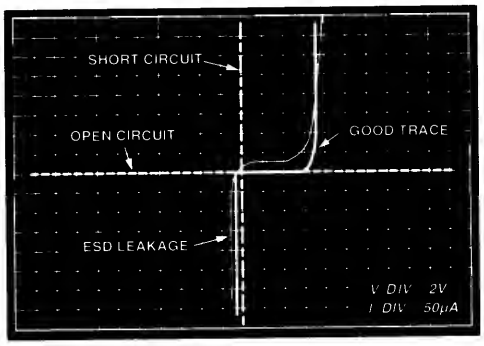

Figure 7. Example of an Unpowered Curve Trace Analysis of a Digital Pin versus a Supply Pin (V_{SS})

LATCH-UP

Latch-up is a potentially destructive situation in which a parasitic active device is triggered, shorting the positive and negative supplies together. If current flow is not limited, electrical overstress will occur. The classic case of latch-up occurs in CMOS output devices, in which the driver transistors and wells form a *pnpn* SCR structure when one of the two parasitic base-emitter junctions is momentarily forward biased during an overvoltage event. The SCR turns on and essentially causes a short between V_{DD} and ground.

Triggering Mechanisms

There are two main triggering mechanisms. *First*, if the input/output (I/O) pin voltage is raised above the positive supply, or lowered below the negative supply, one of the parasitic transistors is turned on. The current returning to the supply through the collector causes a voltage drop across the base-emitter of the second parasitic transistor. In turn, the collector current of the second transistor maintains a forward bias on the base-emitter of the first transistor. If the product of the two transistor gains is greater than unity, the condition may be self-sustaining and can persist even after the external voltage is removed.

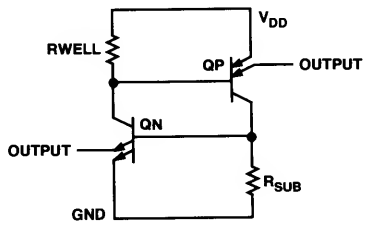

Figure 8. Parasitic SCR. The Diffusions in a CMOS output form a parasitic SCR. The resistors are labeled for an n-well process.

This triggering mechanism can occur if excessive voltage overshoot is present at the I/O pin, or if the signal arrives at the input before the power supplies are applied to the device, or due to electrostatic discharge. This latch-up is usually limited to the devices directly connected to the pin.

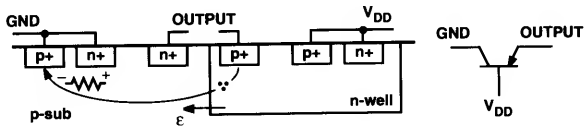

Figure 9a. Output Overvoltage Triggering. Initial hole current flows when the output voltage is raised above V_{DD}. This current causes a voltage rise in the substrate under the NMOS device.

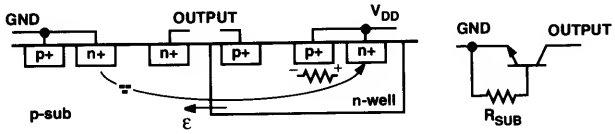

Figure 9b. Current Multiplication. The substrate voltage rise actively biases the second parasitic transistor into conduction. The electron current subsequently causes a voltage drop in the n-well, further turning on the first transistor. If the product of the current gains is larger than one, the final current flow between the supplies can be self-sustaining, limited only by internal resistance's, i.e., an SCR.

Although triggering is by an overvoltage event (typically of only a diode drop above or below the power supplies), the industry practice is to classify the I/O susceptibility in terms of the amount of excess current the pin can source or sink in this overvoltage condition before the internal parasitic resistance's develop enough voltage drop to sustain the latch-up condition. A value of 100 mA is generally considered adequate, with 200 mA considered immune to latch-up.

The *second* triggering mechanism occurs if a supply voltage is raised enough to break down an internal junction, injecting current into the SCR previously described.

This triggering mechanism can occur due to supply transients, or electrostatic discharges shunted to a supply rail. Unlike the case of I/O triggering, latch-up can occur anywhere on the die and is not limited to the vicinity of the external power connections or I/O pins.

The susceptibility to power supply overvoltage is usually limited by the fabrication process on which the device is manufactured, and can be found in the data sheet under the Absolute Maximum Rating specification. If this rating is exceeded, permanent EOS damage may occur. Operating a device near the maximum ratings may degrade the long term reliability of the device. Also the electrical specifications are applicable only at the supply specified on the data sheet and will not be guaranteed above these ratings.

Design Rules

The following is a set of rules to be followed for all designers using CMOS and Bipolar-CMOS ICs:[5]

1. Digital inputs and outputs should not be allowed to exceed V_{DD} by more than 0.3 volts at any time. This includes a power-down situation when V_{DD} = 0 volts.
2. Digital inputs and outputs should also not be allowed to go below DGND by more than –0.3 volts.
3. For mixed signal devices, DGND should not be allowed to exceed AGND by 0.3 volts.
4. For a CMOS or Bipolar-CMOS DAC, I_{OUT} should, in general, not be allowed to drop below AGND by more than 0.3 volts. Some DACs can tolerate significant I_{OUT} current flow, however, without any danger of latch-up.

Latch-Up Prevention Techniques

The following recommendations should be implemented in general, for all applications with CMOS and Bipolar-CMOS ICs that violate one or more of the previously discussed rules:

1. If the digital inputs or outputs of a device can go beyond V_{DD} at any time, a diode (such as a 1N914) connected in series with V_{DD} will prevent SCR action and subsequent latch-up. This works because the diode prevents the base current of the parasitic lateral-PNP transistor from flowing out the V_{DD} pin, thus preventing SCR triggering. This is shown in Figure 10.

   Diodes are also a reliable solution if power-up sequencing is identified as the failure mechanism. In such a case, the insertion of a Schottky diode between the logic inputs and the V_{DD} supply rail (the anode of the diode connected to the logic inputs), will ensure that the logic inputs do not exceed the V_{DD} supply by more than 0.3 volts, thus preventing latch-up of the device.

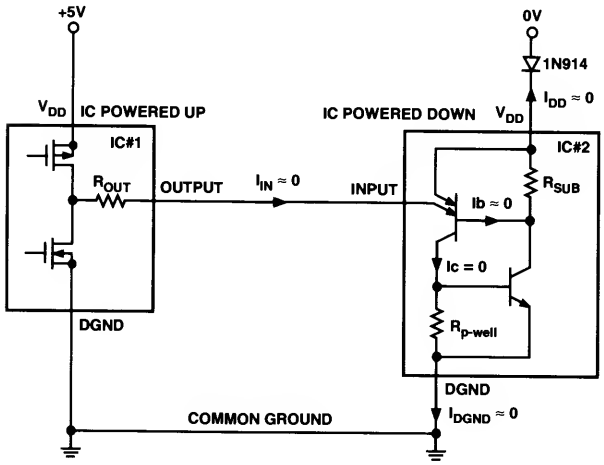

Figure 10. Adding an inexpensive silicon diode in series with the V_{DD} pin of the unpowered IC effectively prevents the parasitic lateral-PNP transistor's base current from flowing and inhibits SCR action.

However, the one *exception* to this rule is when the input range of a device exceeds the supply voltage range of the device, e.g., by design the AD7893-10 12-bit A/D subsystem, the input range is ±10 V and the supply is +5 V.

2. If the digital inputs and outputs of a device can go below DGND at any time, a Schottky diode (such as an HP5082-2835) connected from those inputs or outputs to DGND will effectively clamp negative excursions at –0.3 volts to –0.4 volts. This prevents the emitter-base junction of the parasitic NPN transistor from being turned on, and also prevents SCR triggering. Figure 11 shows the connections for the Schottky diodes.

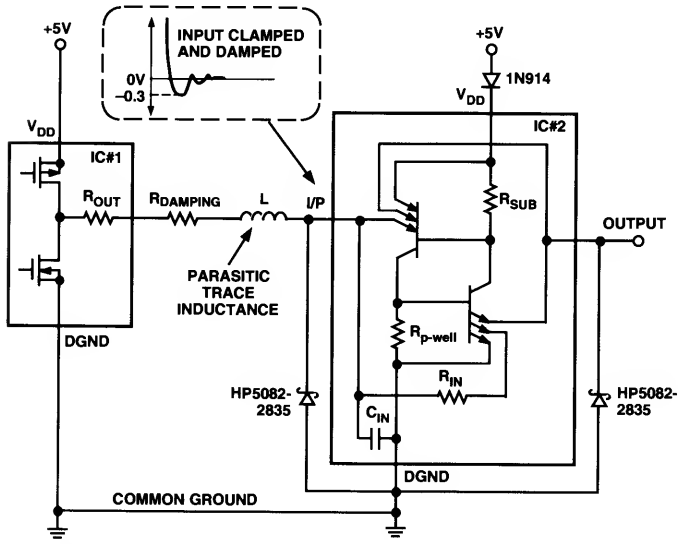

Figure 11. Adding Schottky diodes from the inputs and outputs of a CMOS IC to DGND protects against undervoltages causing conduction of the parasitic NPN, thus inhibiting SCR action. The series damping resistor makes ringing due to long PC board traces die out more quickly.

3. If the DGND potential can occasionally exceed AGND by more than 0.3 volts, a Schottky diode placed between the two pins of the device will prevent conduction of the associated parasitic NPN transistor. This provides additional protection against latch-up as shown in Figure 12. An extra diode connected in inverse parallel with the one just mentioned provides clamping of DGND to AGND in the other direction and will help to minimize digital noise from being injected into the IC.

To identify over- and under-voltage events as described in points (2) and (3) above, the use of a storage oscilloscope is suggested, set at the maximum ratings specification for each pin. Set the Time/Div. to the minimum setting on the oscilloscope (preferably in the ns range). This test should be conducted over a long period of time, e.g., overnight.

4. In circuits where the I_{OUT} pin of a CMOS IC can be pulled below AGND, another Schottky diode clamp between these two terminals will prevent sensitive

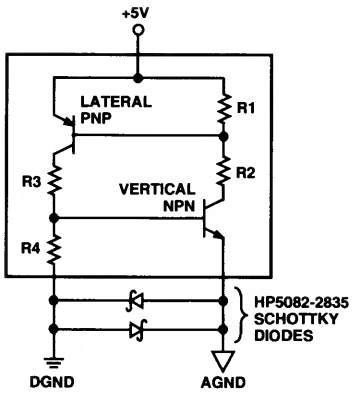

Figure 12. Connecting Schottky diodes between DGND and AGND prevents conduction of the parasitic NPN transistor, and helps to minimize injected noise from DGND to the analog output.

ICs from latching up. This condition sometimes occurs with high speed bipolar operational amplifiers that are used as current-to-voltage converters following a DAC. During power-up or power-down transitions, the op amp's inverting input presents a low impedance from I_{OUT} to the negative supply rail. An unprotected DAC may fail without the recommended Schottky diode clamp to AGND.

5. In designs that have long digital PC board traces between components and are therefore prone to inductive ringing problems, a series damping resistor of 10 Ω–100 Ω will be beneficial. This resistor increases the damping factor of the equivalent series RLC network and causes the ringing to decay more quickly. This will help to prevent conduction of the input or output protection diodes.

High Voltage Transients

If power supply overvoltaging is identified as the failure mechanism, a reliable solution is the insertion of a TransZorb* transient voltage suppressor (TVS). What is a TVS and how does it work?

Transient voltage suppressors[6] (TVSs) are devices used to protect vulnerable circuits from electrical overstress such as that caused by ESD, inductive load switching and lightning-induced line transients. Within the TVS, damaging voltage spikes are limited by clamping or avalanche action of a rugged silicon pn junction which reduces the amplitude of the transient to a nondestructive level.

In a circuit, the TVS should be "invisible" until a transient appears. Electrical parameters such as breakdown voltage (V_{BR}), standby (leakage) current (I_D), and capacitance should have no effect on normal circuit performance.

To limit standby current and to allow for variations in V_{BR} caused by the temperature coefficient of the TVS, the TVS breakdown voltage is usually 10% above the reverse standoff voltage (V_R), which approximates the circuit absolute maximum operating voltage. When a transient occurs, the TVS clamps instantly to limit the spike voltage to a safe level, called the clamping voltage (V_C), while conducting potentially damaging current away from the protected component.

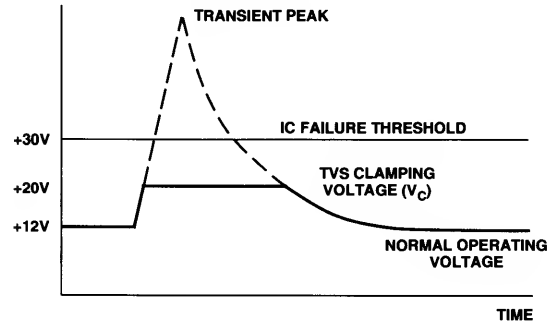

Figure 13. Transients of several thousand volts can be clamped to a safe level by the TVS.

TVSs are designed, specified and tested for transient voltage protection, while a Zener diode is designed and specified for voltage regulation. Therefore, for transient protection the TVS should be selected over the Zener.

The surge power and surge current capability of the TVS are proportional to its junction area. Surge ratings for silicon TVS families are normally specified in kilowatts of peak pulse power (P_P) during a given waveform. Early devices were specified with a 10/1000 μs waveform (10 μs rise to peak and 1000 μs exponential decay to one half peak), while more recent devices are rated for an 8/20 μs test waveform. Power ratings range from 5 kW for 10/1000 μs, down to 400 W for 8/20 μs. This power is derived from the product of the peak voltage across the TVS and the peak current conducted through the device.

TVSs have circuit operating voltages available in increments from 5 V up to 376 V for some families. Because of the broad range of voltages and power ratings available (as well as the universal presence of transient voltages), TVSs are used in a wide variety of circuits and applications.

As an example, consider a pressure transducer which operates at 28 V, placed in an environment in which it encounters a transient voltage of 140 V peak, having a source impedance of 2 Ω and a duration of 10/1000 μs. The failure threshold of the transducer is 40 V, therefore the TVS must clamp at 40 V or less. The current delivered by this transient is:

$$I = (140\ V - 40\ V)/2\ \Omega = 50\ A$$

Note that the voltage clamping action of the TVS results in a voltage divider whereby the open circuit voltage of the transient appears across the combination of the source impedance and the TVS device. Thus the TVS

*TransZorb is a registered trademark of General Semiconductor Industries, Inc.

clamping voltage is subtracted from the transient voltage leaving a net source voltage of 100 V. When the clamping voltage is high compared to the transient peak voltage, the current is significantly reduced.

This circuit can be protected with a 5 kW rated TransZorb TVS which will easily sustain the surge current.

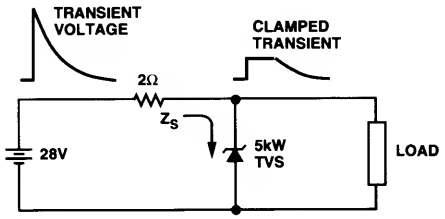

Figure 14. A 5 kW TVS is required to handle the surge current.

An alternate and more economical approach is to add a series resistor to effectively increase the source impedance thus limiting surge current as illustrated in Figure 15. Since the current drawn by the transducer under normal operation is small (<20 mA typical), performance is not adversely affected by a reduction in supply current.

For a small load current, 10 mA, the voltage drop across the added resistance is minimal, about 250 mV for a 25 ohm resistor. Adding this resistor reduces the surge current to:

$$I = (140\ V - 40\ V)/(2\ \Omega + 25\ \Omega) = 3.7\ A$$

This is less than one-tenth the surge current without the resistor. A TVS with lower power rating is able to handle the resulting current. In this case a 500 W suppressor replaces the 5 kW device, saving board space and cost.

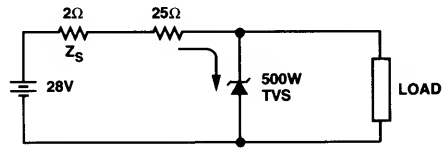

Figure 15. The series resistor reduces transient current allowing a much smaller TVS to be used.

Carbon composition resistors are recommended for this application because of their energy dissipation capability. Steady state power dissipated by the resistor (V×I) is 2.5 mW requiring the lowest rated resistor available for adequate margin.

TYPICAL TVS APPLICATIONS

DC Line Applications

TransZorb TVSs on power lines prevent IC failures caused by transients, power supply reversals or during switching of the power supply between on and off (Figure 16).

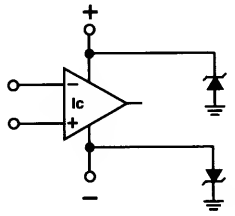

Figure 16.

For power sources utilizing the TransZorb TVS, the TransZorb TVS is chosen such that the reverse stand-off voltage is equal to or greater than the dc output voltage. For certain applications it may be more desirable to replace the series resistor (R) with an inductor (Figure 17).

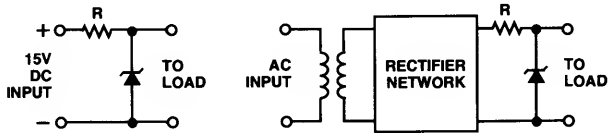

Figure 17.

Signal Line Applications

Input pins are vulnerable to low energy, high voltage static discharges or crosstalk transmitted to the signal wires. Limited protection is provided by the clamp diode or an input network within the IC substrate (Figure 18).

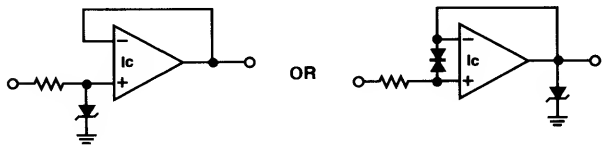

Figure 18.

Transients generated on the line can vary from a few microseconds to several milliseconds in duration and up to 10,000 volts in magnitude. Excess current passing through the diode can cause an open circuit condition or a slow degradation of the circuit performance. TransZorb TVSs located on the signal line can absorb this excess energy (Figure 19).

Figure 19.

A further reference on the subject of using TransZorbs for circuit protection is Analog Devices Application Note AN-311, entitled "How to Reliably Protect CMOS Circuits against Power Supply Overvoltaging."

IN SUMMARY

Designing an application with maximum protection of the integrated circuits is a challenging problem with a solution that depends on many factors. The following is a brief summary of the protection schemes discussed in this application note:

1. Personnel should be trained in the proper handling techniques for prevention of EOS/ESD damage.
2. A good facilities ground system including shielding of equipment and data lines should be implemented.
3. Use transient suppressors judiciously, i.e., check if there are spikes on the supply and the ground lines which may exceed the maximum ratings of those pins.
4. Review the proper power-up sequence of the device(s). The correct order should normally be: GND, Main supplies (if possible the substrate supply being first), V_{CC}, $V_{REF+/-}$ and finally all other pins.
5. Review the data sheet, in particular the maximum ratings section.

Remaining devices from a lot that may have been mistested or subjected to the same conditions as those of any failing devices should be evaluated to determine if latent damage may be present. This analysis should be performed due to the possibility that overstress conditions existed which did not cause immediate failure but induced subtle damage that could result in long-term reliability problems.

Finally, the issue of input overvoltage protection for amplifiers is not discussed in this application note. However, it is exclusively discussed in two other Analog Devices publications; (1) Joe Buxton, "Simple Techniques Protect Amplifiers from Input Overvoltage," *Analog Dialogue* 28-3, 1994, and (2) Joe Buxton, "Input Overvoltage Protection," *System Applications Guide*, Analog Devices, 1993, pp 1–56 to 1–74.

REFERENCES

[1]Henry Domingos, "Circuit Design for EOS/ESD Protection," Proc. 1982 EOS/ESD Symp., pp. 1–17 to 1–21.

[2]John A. Schmidt, Manager of Technical Services IMCS Corporation, Santa Clara, CA, "CDM–The Newest ESD Test Model," 1991.

[3]MIL-STD-883 Method 3015, "Electrostatic Discharge Sensitivity Classification," Military Standard Test Methods and Procedures for Microelectronics.

[4]*ESD Prevention Manual*, 1986. Norwood MA; Analog Devices Inc., pp 9-11. Contains additional references.

[5]Mark Alexander, "Understanding and Preventing Latch-Up in CMOS DACs," AN-109. Free from Analog Devices, PMI Division.

[6]*General Instrument, Power Semiconductor Division Data Book/11th edition*, pp. 633, 696–703. Contains additional references.

Andrew Olney, Analog Devices, Inc., personal communication

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A Guide to Applying and Measuring Operational Amplifier Specifications

By Ray STATA, of *Analog Devices*

Since there are no established standards for operational amplifier specifications we shall discuss the terms used to define operational amplifier characteristics as well as the limitations which must be observed in applying the published data to actual circuits. The test circuits used to measure these parameters are shown. Although these test circuits are applicable to a wide range of operational amplifiers, special amplifiers such as FET, chopper-stabilized or ultra-fast response amplifiers may require changes in the recommended circuit values or in some cases different test methods to measure their specifications. As a general rule the power supply for these measurements should have line and load regulation of about 0.1% and ripple should be no more than a few millivolts.

Figure 1 gives a simplified equivalent circuit for an operational amplifier showing many of the sources of error which are discussed in the text. The specifications should be referenced to this diagram to predict their effect in a closed loop circuit. For a single-ended amplifier you would assume that the plus or non-inverting input is grounded.

Open Loop Gain

Open loop gain, A, is defined as the ratio of output voltage to error voltage $e\varepsilon$ between inputs as shown in Figure 1. Gain is usually specified only at d.c. (A_o), but in many applications such as a.c. amplifiers the frequency dependence of gain is also important. For this reason the typical open loop gain response is published for each amplifier. The open loop gain response of most amplifiers can be approximated by Figure 2.

Open loop gain changes with load impedance (R_L), ambient temperature and supply voltage. As a rule, open loop gain will not change more than a factor of 10 between rated load and no load conditions. Most operational amplifiers have a positive gain temperature coefficient of about 0.5 to 1%/°C and gain changes with supply voltage at about 2%/%. The manufacturer specifies all open loop gains at rated load, 25°C and rated supply voltages.

A practical circuit for measuring open loop gain over a range of frequencies is shown in Figure 3. The voltage divider on the negative input boosts the sensitivity of the error voltage by 100 times which makes it possible to measure gains up to one million. At low frequencies open loop gain is constant so that d.c. gain can be measured by a low frequency signal (about 5 Hz). The voltage divider may not be necessary for low gain amplifiers (below 20000) and it is not recommended for measuring gain at high frequencies where open loop gain is less.

At very best, noise pick-up is a problem for measuring high gains and care must be taken to adequately shield the test circuit. At high frequencies the amplitude of the output voltage must be reduced to avoid exceeding the slewing rate of the amplifier. For this reason the output voltage should be adjusted, so that e_x (peak) < slew rate/ω_1, where ω_1 is the test frequency.

Significance of Open Loop Gain

Operational amplifiers are rarely used open loop. Instead negative feedback is used around the amplifier to improve the accuracy of the circuit. This introduces a second term, closed loop gain (G), which is defined as the gain of the circuit with feedback. The simple inverting amplifier in Figure 4 illustrates this point.

Linearity, gain stability, output impedance and gain accuracy are all improved by the amount of feedback. Figure 5 graphically illustrates the relation between open loop gain and closed loop gain.

The excess of open loop gain over closed loop gain is called loop gain. (Subtraction of dB is equivalent to arithmetic division.) The improvement of open loop performance due to feedback is directly proportional to loop gain. As a general rule for moderate accuracy, open loop gain should be 100 times greater than the closed loop gain at the frequency, or frequencies, of interest (that is loop gain = 100). For higher accuracy, loop gain should be 1000 or more. To illustrate, we recall that open loop gain stability for most operational amplifiers is about 1%/°C. With loop gain of 100, closed loop gain stability would be 100 times better or 0.01%/°C. Likewise, closed loop output impedance would be 100 times less than open loop output impedance with a loop gain of 100.

Rated Output Voltage and Current

Rated output voltage, E_o, is the maximum peak output voltage which can be obtained at rated output current before

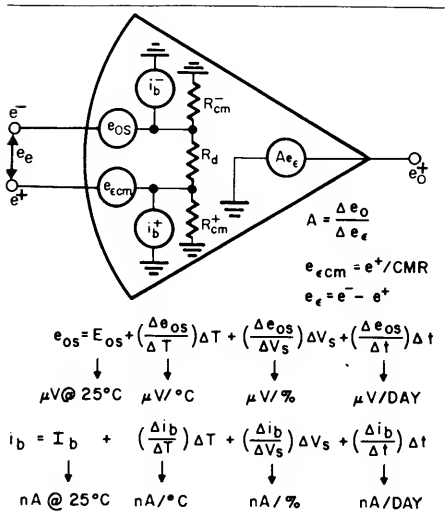


Fig. 1

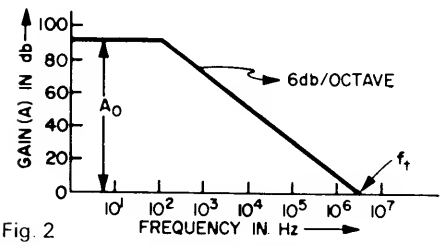


Fig. 2

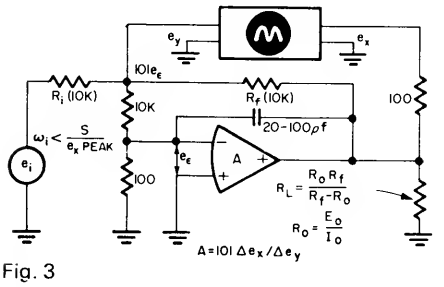


Fig. 3

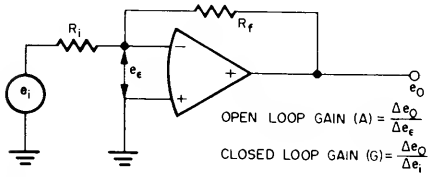


Fig. 4

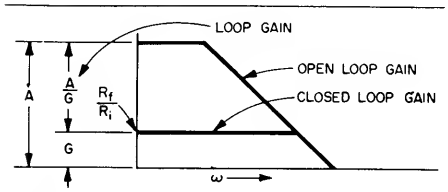


Fig. 5

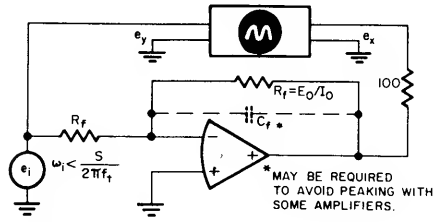


Fig. 6

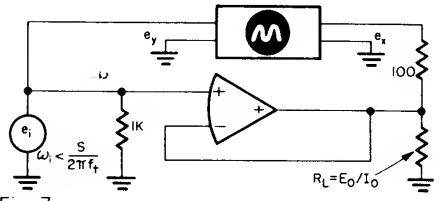


Fig. 7

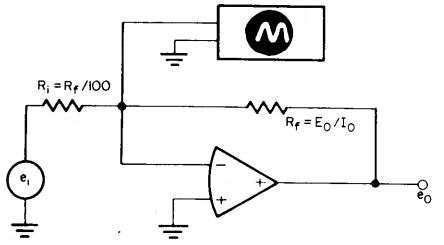


Fig. 8

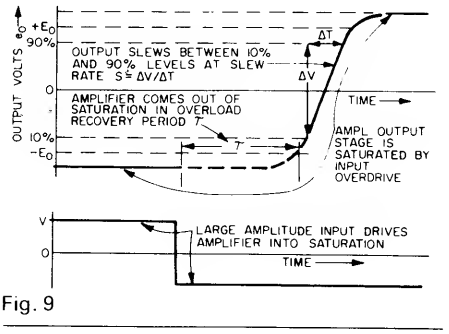


Fig. 9

Fig. 1
Operational amplifier equivalent circuit.

Fig. 2
Typical open loop gain response.

Fig. 3
Open loop gain test circuit.

Fig. 4
Closed loop circuit.

Fig. 5
Determination of loop gain.

Fig. 6
Inverting circuit for measuring f_t, f_p, S, T.

Fig. 7
Non-inverting circuit for measuring f_t, f_p, S, T, E_{cm}.

Fig. 8
Measuring full power response.

Fig. 9
Overload recovery and slew rate illustration.

clipping or excessive non-linearity occurs. This measurement is made at rated power supply voltage; at other supply voltages the output will swing to within about 4 volts of the supply voltage. Also the output voltage swing will increase somewhat at lower load current. Rated output current, I_o, is the minimum guaranteed value of current at the rated output voltage. Load impedance less than E_o/I_o can be used but E_o will decrease, distortion may increase and open loop gain will be reduced. Driving large capacitance loads at high frequencies will present a low load impedance which may then exceed the rated output current. Any convenient circuit such as Figure 3 or Figure 6 can be used to measure E_o and I_o.

Unity Gain Small Signal Response

Unity gain small signal response, f_t, is the frequency at which the open loop gain becomes unity or zero dB (see Figure 2). "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting. Therefore in both measuring f_t and using the amplifier at high frequencies, the output voltage swing must be restricted to avoid slew rate limiting. This implies that the peak output voltage, e_o, for a sinusoidal signal at the unity gain frequency, f_t, must be less than $S/2\pi f_t$, where S is the slew rate.

For amplifiers with symmetrical response on each input, f_t may be measured by either the inverting circuit of Figure 6 or the non-inverting circuit of Figure 7. Some units such as chopper-stabilized amplifiers or wideband amplifiers with feed forward design have fast response only on the negative input which restricts testing and use to the inverting circuit. Remember that the closed loop unity gain response of Figure 6 will be about half the open loop unity gain response due to the loading of the feedback network. Moreover, large values of feedback resistance when coupled with stray capacitance may reduce the closed loop response and therefore the smallest possible value of R_f should be used, the limit being set by output current capability I_o.

Sometimes f_t is called unity gain-bandwidth product which implies that open loop gain at other frequencies can be predicted from this number. However, gain-bandwidth product is constant only

for amplifiers with 6 dB/octave roll off! For fast roll-off amplifiers, gain-bandwidth product increases with gain and thus we publish the open loop response curve to give typical gain at each frequency.

Full Power Response

The large signal and small signal response characteristics of operational amplifiers differ substantially due to dynamic non-linearities or transient saturation. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict. The most prominent contributor to large signal response limitations is slew rate limiting in the output stages. Circuit and transistor capacitances can be charged and discharged only so fast due to the limited dynamic range of the driving circuits. Transient saturation can also occur in the input stages of the amplifier due to overloading the input stage or due to common mode voltage slew rate limiting, but this is rarely a problem as compared with saturation of the output stages.

Full power response, f_p, is the maximum frequency measured at unity closed loop gain, for which rated output voltage, $\pm E_o$, can be obtained for a sinusoidal signal at rated load without distortion due to slew rate limiting. Note that this specification does not relate to "response" in the sense of gain reduction with frequency. Instead it refers only to distortion in the output signal caused by slew rate limiting. For a sinusoidal signal, the maximum slope or rate of voltage change occurs at zero crossing and is proportional to the peak amplitude and the frequency. Thus we see that to a first approximation slew rate, S, and full power response, f_p, are related by equation 1.

$$\left(\frac{de_o}{dt}\right)_{max} = 2\pi f_p E_o = S$$

As the voltage swing is reduced below rated output, E_o, the operating frequency can be proportionally increased without exceeding the slew rate, S. In the limit the operating frequency approaches the unity gain bandwidth, f_t, and the corresponding voltage signal defines the maximum peak amplitude for "small signal" unity gain response. The circuits of Figure 6 or Figure 7 can be used to measure full power response depending on whether inverting or non-inverting parameters are measured. Where dynamic saturation of the output stages is the primary cause for slew rate limiting either test circuit will give equivalent results. For very fast response amplifiers, load capacitance and/or capacitance from the output to the negative input will cause apparent slew rate limiting and consequent degradation of full power response. This is due to saturation of amplifier output current in charging these capacitances and therefore such capacitances must be low.

Output distortion can be measured either by a distortion meter on the output or by observing a Lissajous pattern on an oscilloscope. There is no industry-wide accepted value for the distortion level which determines the full power response limitation, but a number like 1% to 3% is a reasonable figure. One subtle point here is that closed loop output distortion depends on the amount of feedback or loop gain and therefore it depends on the closed loop gain of the measurement. Full power response is generally measured at unity gain where loop gain is the highest. At higher closed loop gains output distortion will increase for the same full power response frequency.

In many applications the additional distortion which is caused by exceeding the full power response can be comfortably ignored. However, a far more serious effect, often overlooked, is that a d.c. offset voltage can be generated when the full power response is exceeded due to rectification of the asymmetrical feedback waveform or due to overloading the input stage with large distortion signals at the summing junction.

These more subtle points in measuring full power response as well as the attendant side effects suggest the circuit of Figure 8 as a more satisfactory test circuit. By viewing the error voltage at the summing junction on an oscilloscope, distortion signals are more easily detected, signal generator distortion is eliminated from the measurement and frequency dependent d.c. offset can be readily observed.

Slewing Rate

The origins of slewing rate limitations were discussed in the previous section. Slewing rate, S, usually expressed in volts/μsec, defines the maximum rate of change of output voltage for a large step change.

Equation 1 suggests a convenient method to measure slewing rate by first measuring full power response, f_p, and then calculating S. Although this test method yields usable results for most amplifiers in most applications, the relationship of equation 1 does not apply under all conditions. First, slewing rate is a non-linear function of output voltage and equation 1 measures slewing rate only at zero volts output. This second-order effect can usually be safely ignored in most applications. However, for certain amplifiers, particularly fast response types, the slew rate may be higher than that predictable from f_p. In these cases f_p is limited by factors other than slew rate such as d.c. offset errors which are generated by the rectification of large high-frequency error voltages.

A more direct method to measure slewing rate is to apply low-frequency square waves (about 100 Hz) to the input of Figure 6 or Figure 7 which cause full voltage swing at the output and to observe the rise time from 10 to 90% on an oscilloscope (see Figure 9). Small feedback resistors must be used to avoid degradation of slewing rate due to stray capacitance.

In applying operational amplifiers remember that repetitive input waveforms whose rise time exceeds the amplifier's slewing rate will generate voltage spikes at the summing junction. These spikes are usually asymmetrical and are also usually clipped asymmetrically by the input circuit of the amplifier—either or both of which effects will cause d.c. offsets at the output.

Overload Recovery

Overload recovery, τ, defines the time required for the output voltage to recover to the rated output voltage E_o from a saturated condition. For this test the circuit of Figure 6 or 7 is used with an input square wave adjusted to be 50% greater than the voltage required to saturate the amplifier output. The square-wave frequency should be adjusted to about 100 Hz and the input-output signals should be compared on a dual trace oscilloscope as illustrated in Figure 9.

In some amplifiers the overload recovery will increase for large impedances (greater than 50 KΩ) in the input circuit, either the summing impedance for Figure 6 or the source input for Figure 7. Published specifications apply for low

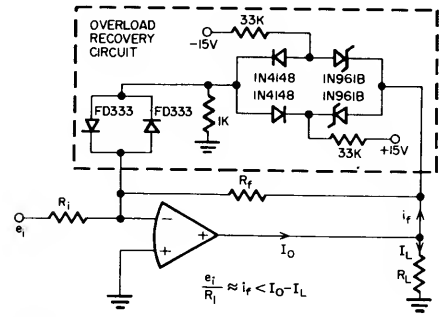
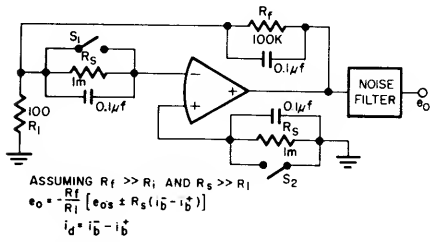


Fig. 10



Parameter	Switch Position S1	S2	Output Voltage
e_{os}	Closed	Closed	$e_o = -(\frac{R_f}{R_i})e_{os}$
i_b^-	Open	Closed	$e_o = -(\frac{R_f}{R_i})R_s i_b^-$
i_b^+	Closed	Open	$e_o = -(\frac{R_f}{R_i})R_s i_b^+$
i_d	Open	Open	$e_o = -(\frac{R_f}{R_i})R_s i_d$

Fig. 11

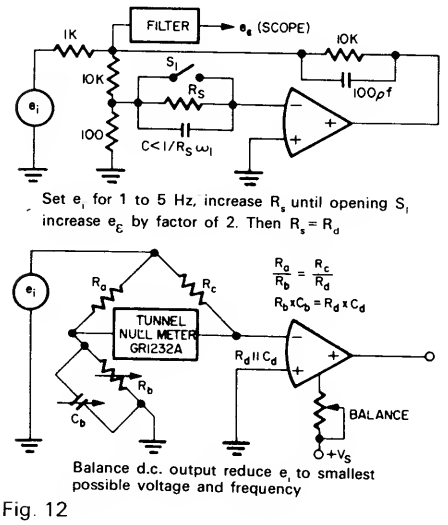


Fig. 12

Fig. 10
External clamp circuit for ±10 volts.

Fig. 11
Test circuit for offset voltage, bias current and difference current.

Fig. 12
Differential impedance test circuits.

impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network.

Normally, overloaded recovery time runs about one millisecond. For the inverting configuration an external clamp circuit can be added to improve overload recovery as illustrated in Figure 10. This circuit prevents the output from saturating and therefore circumvents any delays due to overload recovery. The only constraint for proper operation is that input current (e_i / R_i) shall be approximately less than the rated output current I_o minus the load current. The clamp circuit cannot be used with the non-inverting and differential configurations.

Initial Offset Voltage

Offset voltage, e_{os}, is defined as the voltage required at the input from a zero source impedance to zero the output, at any temperature, supply voltage and time (see Figure 1). Initial offset voltage, E_{os}, defines the offset voltage at 25°C and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer. Some amplifiers are internally trimmed to guarantee some maximum limit on initial offset (usually ±1mV) which means that in certain applications the external trim pot can be eliminated. On special order any amplifier from the manufacturer can be internally trimmed to ±1mV initial offset or less. Initial offset can be measured with the circuit of Figure 11, where an appropriate fixed resistor is substituted for the external trim potentiometer. There is a warm-up drift of offset voltage following the application of power supply voltage and it is recommended that you let the amplifier stabilize for at least 15 minutes before making measurements.

Initial Bias Current

Bias current, i_b, is defined as the current, at any temperature, supply voltage and time, required at either input from an infinite source impedance to zero the output assuming zero common mode voltage. For differential amplifiers bias current is designated by i_b- for the negative input and by i_b+ for the positive input. For single-ended amplifiers, like chopper-stabilized units, bias current refers to the current at the negative input only.

Initial bias current, I_b, is the bias current at either input measured at 25°C, rated supply voltages and zero common mode voltage. The designation (0,+) or (0,−) indicates that no internal compensation is used to reduce initial bias current so that the polarity is always known. The sign tells to which power supply voltage an external compensating resistor should be connected to zero the initial bias current. The designation (±) indicates that internal compensation has been used to reduce initial bias current and that the residual bias current can be of either polarity. In general, compensating initial bias current has little effect on the bias current temperature coefficient. The circuit of Figure 11 is used to measure initial bias current.

Initial Difference Current

Difference current, previously called offset current, i_d, is defined as the difference between the bias currents at each input from an infinite source required to zero the output assuming zero common mode voltage. The input circuitry of differential amplifiers is generally symmetrical so that bias current at each tends to be equal and tends to track with changes in temperature and supply voltage. Usually difference current is 3 to 5 times less than bias current at either input, assuming that initial bias current is not compensated. If the impedance as seen from each input terminal to ground is balanced then offset and drift errors are proportional to difference current rather than to bias current. In most applications, if the external impedances at each input are balanced then there is no particular advantage in using an amplifier where initial bias current is internally compensated. Initial difference current, I_d, the difference current measured at 25°C and rated supply voltage, can be measured by the circuit of Figure 11.

Temperature Drift

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. By far this is the most important source of error in most applications. The temperature coefficients of these parameters, $\Delta e_{os}/\Delta T$, $\Delta i_b/\Delta T$ and $\Delta i_d/\Delta T$ are all defined as the average slope over a specified temperature range and are determined by subtracting the offset values at the end

points of the temperature range and dividing by the temperature change. In general, drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal room ambient. The temperature drift coefficients are measured by the circuit of Figure 11. The amplifier is used to boost its own low level input offset signal to a conveniently measurable voltage at the output. Gain is established by the ratio of R_f/R_i. The current sampling resistors, R_s, must be selected so that voltage drift is small compared with the drift due to difference current; that is $R_s \times \Delta i_d/\Delta T >> \Delta e_{os}/\Delta T$. Alternatively, voltage drift must be subtracted from the data for current drift.

One problem in using published voltage drift specifications is that these data apply only to static temperature conditions where the temperature of the module is assumed to be uniform. Voltage offset of most differential amplifiers is quite sensitive to thermal gradients, since drift performance depends on the cancellation of large offset in each transistor of the input differential pair. Therefore in environments where thermal gradients are present voltage offset may exceed that predictable from the drift coefficients. In this case where low drift over a narrow temperature range is critical, it is good practice to insulate or shield the amplifier to assure a uniform temperature. Bias current is not noticeably affected by thermal gradients and difference current, while affected, is far less sensitive to gradients than voltage offset.

Bias current and difference current for FET and varactor bridge amplifiers double each 10°C and therefore a linearized drift coefficient has little meaning except over a narrow operating temperature range.

Supply Voltage Sensitivity

Offset voltage, bias current and difference current will also change when supply voltage is varied. Usually errors due to this effect are negligible compared with temperature drift. Static or d.c. supply voltage coefficients, $\Delta e_{os}/\Delta V_s$, $\Delta i_b/\Delta V_s$, $\Delta i_d/\Delta V_s$, are measured with the circuit in Figure 11 by varying supply voltages individually by ± 1 volt.

There is a common misconception that tracking power supplies whose plus and minus voltages change by the same amounts will improve supply voltage coupling. In general tracking supplies are of no benefit since the positive supply voltage coefficient is usually much larger than the negative supply voltage coefficient. Rejection of a.c. noise and ripple on the power supplies is not as good as static or d.c. rejection, but for almost all amplifiers a.c. rejection will be better than 1 mV/V or 60 dB over a wide range of frequencies.

Drift vs Time

Offset voltage, bias current and difference current change with time as components age. Static data over long time periods are difficult to obtain because of the inherent time delays involved. But it is safe to say that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper-stabilized amplifier (which by the way is by far the best amplifier type for long-term stability) is usually quoted as 1 μV/day whereas cumulative drift over 30 days will usually not exceed 5 μV nor 15 μV in a year.

Long-term voltage drift in differential input type amplifiers depends primarily on the aging of collector resistors in the input differential pair. The aging coefficient referred to the input is about 300 μV/% change of collector resistance. It is not unlikely that carbon composition resistors will age by 1 or 2% over a year resulting in an offset voltage change of 300 to 600 μV. The use of metal film resistors for the collector resistors will greatly improve long-term stability to the point where base-to-emitter voltage aging is the determining factor. With metal film resistors, drift of offset voltage for transistor amplifiers is about 100 μV/year while FET amplifiers will age somewhat more.

Long-term bias current stability in differential input amplifiers again depends on resistor stability when internal initial current compensation is employed. In this case, multi-megohm carbon composition resistors are used (since large value metal film resistors are not available) to supply about 90% of the base bias current. If these resistors change by 1%, the specified initial bias current will change by about 9% which can be a substantial drift. Therefore one can conclude that amplifiers without internal initial current compensation will exhibit more stable bias current. Under these conditions long-term bias current stability depends primarily on the stability of the transistor or FET devices which may be better than 1%.

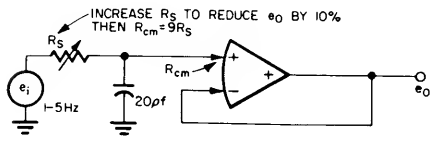


Fig. 13

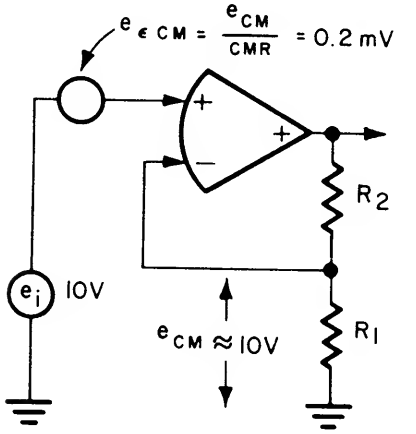


Fig. 14

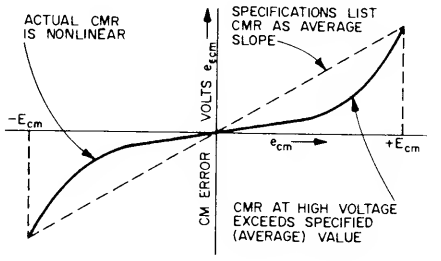


Fig. 15

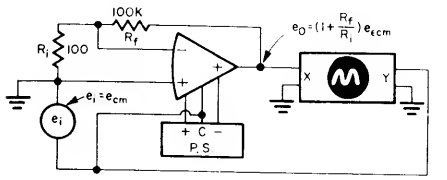


Fig. 16

Fig. 13
Common mode impedance test circuit.

Fig. 14
Illustration of common mode voltage.

Fig. 15
CM error vs CM voltage.

Fig. 16
CMR test circuit.

Input Impedance

Differential input impedance, R_d, is defined as the impedance between the two input terminals, measured at 25°C, assuming that the error voltage, eε, is nulled or very near zero volts (see Figure 1). For a single-ended amplifier, R_d is the input impedance since the plus input is grounded. To a first approximation, dynamic impedance can be represented by a capacitor, C_d, in parallel with R_d.

Differential input impedance is among the most difficult parameters to measure particularly for a high gain, high impedance type amplifier. In general this measurement can only be made under laboratory conditions by an experienced engineer with special fixtures to shield against noise pick-up. For this reason most companies rarely measure this parameter on a production line basis. Fortunately a precise knowledge of R_d is not required, since for most circuits, so long as R_d is large compared with the external feedback impedance, its value has little bearing on closed loop performance.

The circuits of Figure 12 show in principle how R_d can be measured with enough attention to reducing noise. These circuits actually measure R_d in parallel with the negative input common mode impedance. However, common mode impedance is usually 10 to 100 times greater than R_d so that the error is negligible.

Common mode impedance, R_{cm}, is defined as the impedance between each input and ground or power supply common and is specified at 25°C. (See Figure 1.) For most circuits common mode impedance on the negative input, $R_{cm}-$, has little significance except for the capacitance which it adds to the summing junction. However, common mode impedance on the plus input, $R_{cm}+$, sets the upper limit on closed loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor, C_{cm}, in parallel with R_{cm} which usually runs from 5 to 25 pF on the plus input.

The circuit of Figure 13 can be used to measure $R_{cm}+$ up to about 500 M-ohms. Use an oscillator frequency of 1 to 5 Hz and adjust R_s for 10% reduction at the output. Then $R_{cm}+ = 9\ R_s$. Above this impedance it is advisable to substitute a picoameter for the resistor R_s and to measure d.c. bias current as a function of common mode voltage.

Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers common mode impedance is reduced by a factor of two for each 10°C temperature rise.

As a function of common mode voltage, R_{cm} is defined as average impedance for a common mode voltage change from zero to $\pm E_{cm}$, that is, maximum common mode voltage. Incremental R_{cm} about some large common mode voltage may be considerably less than the specified average R_{cm}, especially for FET input amplifiers.

Maximum Voltage between Inputs

Under most operating conditions, feedback maintains the error voltage, eε, between inputs very near to zero volts. However, in some applications, such as voltage comparators, or where the input voltage exceeds the level required to saturate the output, the voltage between inputs can become large. E_d defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier. Placing parallel back-to-back diodes across the input terminals is one way to provide added protection for the amplifier.

Maximum Common Mode Voltage

For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, e_{cm}, is defined as the voltage above ground at each input when both inputs are at the same voltage. E_{cm} is defined as the maximum peak common mode voltage at the input before clipping or excessive non-linearity is seen at the output. E_{cm} establishes the maximum input voltage for the voltage follower connection. (See Figure 7.)

E_{cm} is measured with the circuit of Figure 7 by increasing the peak input voltage (sinusoidal waveform) until distortion is seen on the scope (about 1 to 3%). The input signal frequency must be well below the full power response frequency, f_p, for the non-inverting input.

Common Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs (e+ — e−) and produces no

output for a common mode voltage—that is when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely subtracted at the output. If we refer the output common mode error voltage to the input (dividing by gain) and call this the input common mode error voltage, $e\varepsilon_{cm}$, then common mode rejection (CMR) is defined as the ratio of common mode voltage to common mode error voltage. That is CMR = $e_{cm}/e\varepsilon_{cm}$. CMR is sometimes expressed in dB in which case you take 20 times the log (base 10) of the ratio. Errors due to common mode rejection can be represented in the equivalent circuit of Figure 1 by a voltage generator, $e\varepsilon_{cm}$, in series with the input. Note that common mode error goes to zero when either input is grounded. Therefore the inverting configuration does not exhibit a common mode error since the plus input is grounded. Thus CMR is only a problem in the non-inverting and differential configurations where common mode voltage varies in direct proportion to the input signal. In this case $e\varepsilon_{cm}$ is a basic measuring error which affects the over-all circuit accuracy.

For example, if a 10-volt signal, e_i, were applied to the input of the circuit in Figure 14, common mode voltage, e_{cm}, is equal to the input voltage, e_i. This would cause a common mode error voltage, $e\varepsilon_{cm}$, of 2mV for an amplifier with 5000 or 74 dB CMR and thus a 0.2% measuring error.

Precisely specifying CMR is complicated by the fact that common voltage error, $e\varepsilon_{cm}$, can be a highly non-linear function of common mode voltage and it also varies with temperature. This is particularly true for FET input amplifiers. As illustrated by Figure 15, CMR published by the manufacturer are average figures assuming an end-point measurement at maximum common mode voltage, $\pm E_{cm}$. But the incremental CMR about some large common mode voltage may be less than the average CMR which is specified. In fact, if common mode error were a linear function of common mode voltage and if CMR were not strongly influenced by temperature then this source of error would be of little consequence. This follows since a linear CMR error can be viewed as a gain error which could be compensated for by adjusting the closed loop gain. Therefore linearity of common mode error, $e\varepsilon_{cm}$, vs common mode voltage is actually more important for many applications than CMR itself.

The circuit in Figure 16 provides a unique method to instrument CMR measurements as well as to measure the non-linearity of common mode errors. The oscilloscope display will duplicate the pattern of Figure 15. A floated power supply allows a single-ended oscilloscope to be used and almost any regulated power supply has floated outputs with sufficient isolation. Published CMR specifications apply only to d.c. input signals so that this measurement should be made with a signal frequency of 5 Hz or less. CMR at higher frequencies, although not guaranteed by the specifications, can also be measured with this circuit. It is further assumed that the external circuit impedances of both the test circuit and the application are small compared with the common mode impedance to avoid additional common mode errors due to impedance unbalance.

Input Noise

Input voltage and current noise characteristics can be in principle measured, specified and analysed very much like offset voltage and bias current characteristics. In fact, offset voltage and bias current drift can be considered noise which occurs at very low frequencies. For this purpose in both the equivalent circuit of Figure 1 and the test circuit of Figure 11, replace e_{os} by e_n, an equivalent voltage noise generator, and replace i_b- and i_b+ by i_N- and i_N+, equivalent current noise generators. The primary difference in measuring and specifying noise as opposed to d.c. drift is that bandwidth must be considered. At low frequencies, 100 Hz or less, 1/f noise prevails, which means that the noise per root cycle increases inversely with frequency. At the mid-band frequencies noise per root cycle is constant or "white".

To measure noise a sharp cutoff bandpass filter is added to the output of the circuit of Figure 11. Furthermore the impedance, gain and capacitors must be adjusted to assure that neither the amplifier nor the external feedback components limit the noise bandwidth of the measurement. For very low current noise, it becomes very difficult to make wideband measurements because of the interaction of stray capacitance and the large sampling resistor values needed to boost sensitivity.

Usually two noise measurements are taken. Low frequency noise in a bandpass of 0.01 to 1 Hz is measured on a strip chart recorder and is specified as peak to peak with a 3σ uncertainty, meaning that 99% of the observed peak-to-peak exclusions will fall within the specified limits. Wideband noise in a bandpass of 5 Hz to 50 kHz is measured on a VTVM, preferably a true RMS type, and is specified as rms. Of course, shielding becomes very critical in these measurements to avoid power line frequency and radio frequency pick-up.